This listing of claims will replace all prior versions and listings of claims in the application:

**Listing of Claims**:

Claims 1 (canceled)

Claim 2 (currently amended) The ~~device~~ method of Claim [[1]] 7, wherein said back bias is less than the breakdown voltage of drain-substrate and source-substrate junctions.

Claim 3 (currently amended) The ~~device~~ method of Claim [[1]] 7, wherein said back bias is between about -5 V and about -0.1 V.

Claim 4 (currently amended) The ~~device~~ method of Claim [[1]] 7, wherein said back bias is between about -3V and about -1 V.

Claim 5 (currently amended) The ~~device~~ method of Claim [[1]] 13, wherein said CMOS device ~~is engineered to have~~ has a threshold voltage within a selected operating range while said steady negative ~~voltage~~ back bias is applied.

Claim 6 (currently amended) The ~~device~~ method of Claim 5, wherein said operating range is between 0 V and 0.8 V.

Claim 7 (previously presented): A method for operating a bulk CMOS or NMOS device to resist total dose radiation effects due to charge build up in a field oxide, said method comprising the steps of:

selecting a maximum ionizing radiation dose for operation of said bulk CMOS or NMOS device, wherein said CMOS or NMOS device comprises a Si substrate; two or more FETs on said substrate; a field oxide region separating each FET; a negative voltage source for applying a steady negative back bias to a NMOS region of said substrate and for increasing the threshold

voltage of the field oxide region to reduce leakage currents due to radiation damage in said field oxide region thereby mitigating total dose radiation effects, and wherein a bulk CMOS device does not include an insulator beneath said FETs; and

determining and applying said negative back bias to said substrate of NMOS components of said bulk CMOS or NMOS device, wherein said negative back bias is sufficient to essentially eliminate leakage currents due to total dose radiation in said field oxide region of said CMOS or NMOS device thereby providing hardness against said maximum ionizing radiation dose.

Claims 8-9 (canceled)

Claim 10 (currently amended) The method of claim 7, wherein said CMOS or NMOS device ~~is engineered to have~~ has a threshold voltage within a selected operating range while steady negative ~~voltage~~ back bias is applied.

Claim 11 (currently amended) The method of claim [[10]] 7, wherein said ~~operating range is~~ device has a threshold voltage between 0 and 0.8 V while said steady negative back bias is applied.

Claim 12 (canceled)

Claim 13 (new) A method for resisting total dose ionizing radiation effects in a bulk CMOS or NMOS device, the device having a Si substrate, two or more FETs on the substrate, and a field oxide region separating each FET, the device configured so application of a steady negative back bias to the substrate results in a threshold voltage between about 0 V and 0.8 V,

the method comprising:

placing the device in a radiation environment;

applying the steady negative back bias relative to a source voltage to a MOS region of the substrate.

Claim 14 (new) The method according to Claim 13, wherein said applying the steady negative back bias includes applying about -2V to the MOS region of the substrate, and

the method further including applying about 3.3 V to a gate of the FET relative to the source and a drain of the FET.

Claim 15 (new) The method according to Claim 13, wherein said placing the device in a radiation environment comprises placing the device in a radiation environment of at least about 10 krad.

Claim 16 (new) The method according to Claim 13, wherein said placing the device in a radiation environment comprises placing the device in a radiation environment of between 10 and 200 krad.

Claim 17 (new) The method according to Claim 13, wherein said placing the device in a radiation environment comprises placing the device in a radiation environment of at least about 100 krad.

Claim 18 (new) The method according to Claim 13, wherein said placing the device in a radiation environment comprises placing the device in a radiation environment of at least about 200 krad.